Enhancement of Solar PV Output Error Under Variable Irradiation and Temperature Using an Improved Regulation Strategy

Ayodeji S. Akinyemi
Dept. of Electrical Power Engineering
Durban University of Technology
Durban, South Africa
aystevo@gmail.com

M. Kabeya
Dept. of Electrical Power Engineering
Durban University of Technology
Durban, South Africa
MusasaK@dut.ac.za

Innocent E. Davidson
Dept. of Electrical Power Engineering
Durban University of Technology
Durban, South Africa
lininnocentD@dut.ac.za

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***Abstract*—A Photo-Voltaic Solar System (PVSS) is being operated in Steve Biko campus, Durban University of Technology. The energy generated by the PVSS is time varying, based on the quantity of sunlight and the temperature at which the photovoltaic (PV) cell functions. Consequently, in all situations, it is critical to obtain the full power from the PV array. The monitoring control strategy of Maximum Power Generated (MPG) from the PVSS connected to a Boost Inverter (BI) is presented in this research paper by employing an Improved Incremental Conductance and Integral Regulator (IIC & IR). The outcomes of the simulation indicate that full power can be obtained from the PV array while ensuring a consistent generated voltage under various operating scenarios.**

Keywords—Blocking/Deblocking signal, Inverter restoration, Incremental conductance, Integral regulator, Tracking error

I. INTRODUCTION

This countries across the world' emphasis have shifted to power produced from clean energy sources, that are renewable on a human time scale. The fast growth of human population and the increased consumption of traditional energy sources results in an increase in the demand for more power and better solutions for a safe, non-contaminating atmosphere. Solar power stands out among these Renewable Energy Resources (RES) because of its ease of integration into power systems and operation flexibility in comparison to the traditional methods of energy production [1]. In South Africa, approximately 8.3 GW equivalent power from various types of RES was achieved in 2020, with PVSS accounting for 2.5 GW of this potential [2]. Notwithstanding, this is insufficient; more will be installed all over the country in the near future. Numerous tracking algorithms have recently been explored to obtain maximum output at any given sun irradiance level [3], The Perturb and Observation (P&O) approach is a widely used algorithm due to its easy and speed of implementation; however, the technique's output level fluctuation is a drawback. It could also mistakenly stalk at the point of the highest power produce in the reverse way if the location of the sun's luminance changes quickly [4]. Incremental Conductance (IC) is another technique that has a greater possibility than the P&O techniques. Nevertheless, the procedure has the drawback of limiting performance because it can tilt around the MPG [5], [6], [9], necessitating the development of a IIC & IR algorithm that is strong, balanced, and swing-free. The PVSS is connected to a distribution network at the common point.

This paper proposed a IIC & IR strategy to track MPG with perfect efficiency, time savings, and distortion reduction. The IR is incorporated to reduce the produced error (e) to zero, can also be used to eliminate the fluctuation that exist at MPG with an Instantaneous Conductance (InC) and (IC) to a negligible value i.e., e = 0. The grid inverter is incorporated with blocking and de-blocking arrangement to safeguard the installed power component/equipment from short-circuit signals. PVSS are designed in Simulink software, and IIC & IR is employed to track the MPG from the modules. A BI is required to make sure the optimal output power provision of the PVSS to supply electricity to a consumer at controllable solar insolation and climate. The remaining structure of this article is organized as follows: section 2 explores the PVSS, IIC is described in section 3, section 4 discusses the modelling of the BI, V. Section 5 discusses inverter blocking/de-blocking method, section 6 describes the test system, section 7 presents simulation outcomes and section 8 conclude the paper.

II. PHOTOVOLTAIC SOLAR SYSTEM (PVSS)

Figure 1 depicts PV modules equivalent diagram with parallel/series circuit elements and a diode connected to a current source [7].

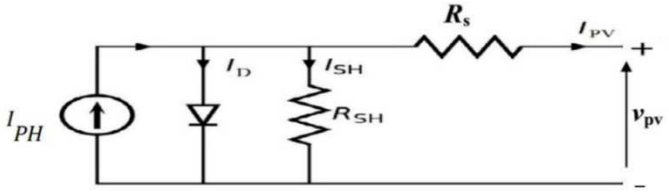

Fig. 1: Solar PV Module Equivalent Circuit.

In Fig. 1, $I_{pv}, V_{pv}, I_{ph}, R_s, I_s, R_p, I_d, V_d$ *and* I_p are the PV parameters while *K*, *T*, *q*, and *A,* having constant values which are defined in appendix A. The Eqs. 1 and 2 representations can be used to calculate the PV current flows through the circuit [8].

$$(\mathrm{I_{PV}}) = \mathrm{I_{ph}} - \mathrm{I_d} - \mathrm{I_p} \quad (1)$$

$$\mathrm{I_{pv}} = \left\{\mathrm{I_{ph}} - \mathrm{I_S}\left(\mathrm{e}^{\frac{q[V_{PV}+R_S I_{PV}]}{AKTN_{SE}}}\right) - 1\right\} - \frac{(R_S I_{PV}+V_{PV})}{R_P N_{SE}} \quad (2)$$

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III. INCREMENTAL CONDUCTANCE (IC)

The IC technique is based on the observation that at the maximum point, the first derivative of the P-V function equals zero, that means $\frac{\partial p}{\partial v} = 0$. The IC method is focused on the consequence of PV power and voltage = 0 at MPP. It finds MPP because conductance $(G = \frac{1}{V})$ and conductance increment $(G = \frac{\Delta I}{\Delta V})$ are equal. Since solar system current is proportional to voltage, solar energy can be generated. So, if eq. 3 equals zero, the MPP is achieved when the IC equals to the negative of the InC, as shown in eq. 8, and the potential difference at that position is referred to as MPP voltage in eq. 9. The system delivers this MPP voltage till the solar irradiation ΔI varies due to atmospheric condition fluctuation.

$$\text{at PPP}, \frac{\mathrm{dP}}{\mathrm{dV}} = 0 \tag{3}$$

$$\mathrm{P} = \mathrm{I} \times \mathrm{V} \tag{4}$$

$$\mathrm{P} = \mathrm{I(V)} \times \mathrm{V} \tag{5}$$

$$\frac{\mathrm{dP}}{\mathrm{dV}} = \mathrm{V} \times \frac{\mathrm{dI}}{\mathrm{dV}} + \mathrm{I(V)} \tag{6}$$

$$\mathrm{V} \times \frac{\mathrm{dI}}{\mathrm{dV}} + \mathrm{I(V)} = 0 \tag{7}$$

$$\frac{\mathrm{dI}}{\mathrm{dV}} = -\frac{\mathrm{I(V)}}{\mathrm{V}} \tag{8}$$

$$\text{at PPP}, \mathrm{V_{ref}} = \mathrm{V_{PPP}} \tag{9}$$

A. IMPROVED IC & IR

As shown in Fig. 4, an IR controller is introduced to the IC for maximum efficiency and time savings when tracking MPP. The distortions produced at MPP between InC and the IC can be derived to zero with the proportional integral approach. Thus, e can be equated to '0' in eq.10.

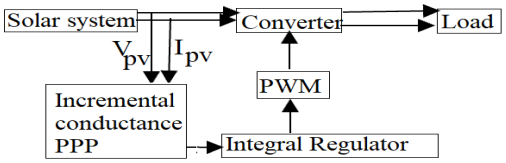


Fig. 4: IIC & IR.

When IR control is introduced to the IIC, the output fluctuation is reduced, resulting in better signal that is free from distortion, continuous process improvement, adjustment of the PV to the weather variation enhances the network performance. When the operational level is far from the PPP, the proportional integral regulator enhances the accuracy of both the system's large step sizes and when the PPP's small step sizes are attained to fully exploit possible level of power. IR restores the controlled variable to its initial state after a distortion at the input and nullifies the offset, which the traditional IC cannot perform. The conventional IC produces an offset because it ignores the error's previous history. The IR controller employs both proportional and integral modes to evaluate performance based on the difference between a measured variable and a set reference.

$$e = \frac{1}{\mathrm{V}} + \frac{\mathrm{dI}}{\mathrm{dV}} \tag{10}$$

IV. BOOST INVERTER (BI) DESIGN

A BI is required for the proper performance of the MPP detection algorithm. A BI is required for enhancing the output power usage of a PVSS under various environmental conditions. The proposed BI and IIC & IR for the MPP approach are shown in Figure 5. The inverter's input inductance is critical for MPP dynamics; thus, it directs the MPP operation and stabilizes the PVSS voltage to precisely suit the voltage at the MPP. The problem of low power output is related to the traditional IC, where MPP advancement is restricted, leading to decreased in tracking effectiveness, which is rectified by the proposed technique. To minimize error, the error signal derived in IC is being attenuated by the IR regulator. Figure 5 shows the proposed IIC & IR algorithm for accessing the PPP using a BI, and its mathematical model of the inverter can be represented in Eqs. 11– 13. When R_b is put into consideration in Figure 5, the Laplace equivalent of the BI is represented by Eq. 14, while eq. 15 provides the total Laplace equivalent of the PVSS [10]. eq. 16 expresses the consistent RI regulator's transfer function.

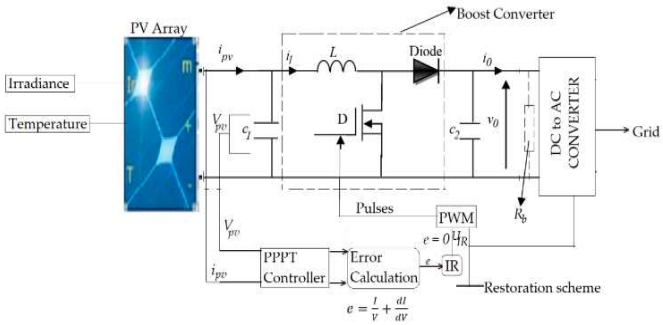


Fig. 5: Proposed BI and the IIC &IR MPP method

$$\frac{\partial v_{pv}}{\partial t} = \frac{i_{pv} - i_l}{C_1} \tag{11}$$

$$\frac{\partial i_l}{\partial t} = \frac{v_{pv} - (1-D)v_0}{l} \tag{12}$$

$$\frac{\partial v_0}{\partial t} = \frac{(1-D)i_l - \left(\frac{v_0}{R}\right)}{C_2} \tag{13}$$

$$G_i(s) = \frac{(V_0 C_2)s + 2.\frac{V_0}{R_b}}{(LC_2)S^2 + \frac{L}{R_b}.S + (1-D)^2} \tag{14}$$

$$G_i(s) = -\frac{\frac{V_0}{LC_1}S + \frac{V_0 + R_b(1-U_{IR})i_l}{R_b LC_1 C_2}(V_0 C_2)s + 2.\frac{V_0}{R_b}}{S^3 + \left(\frac{1}{R_b C_2} + \frac{R}{L}\right)S^2 + \left(\frac{C_2 + C_1(1-U_{IR})^2}{LC_1 C_2} + \frac{R}{R_b LC_2}\right)S + \frac{1}{R_b LC_1 C_2}} \tag{15}$$

$$G_s(s) = K_{pb} + \frac{K_{ib}}{s} \tag{16}$$

A. Proposed Inverter Restoration Strategy

The inverter's blocking and de-blocking control strategy is regarded as an incident energized controller in order to optimize interactions between various controllers. Logic B is the blocking signal at the inverter's input, which is usually minimal or nil, as shown in Fig. 6. When the inverter receives the information, it instantly shuts down. When a fault occurs on the power network, the safety system and disconnector are

perfectly aligned to complete the fault isolation procedure. The inverter detects the fault and sends a blocking signal to the Circuit Breaker (CB), which then isolates the fault. Throughout this time, the inverter functions as a rectifier diode. The proposed inverter control strategy is made up of three modules: the blocking/de-blocking, the sensor, and the automatic de-blocking. The regulate sensor collects, analyses, and re-arranges voltage, current, disconnector, and the inverter data into various types of signals such as incident signals, logic signals, and so on, and then transmits the message to the next segment as a process data.

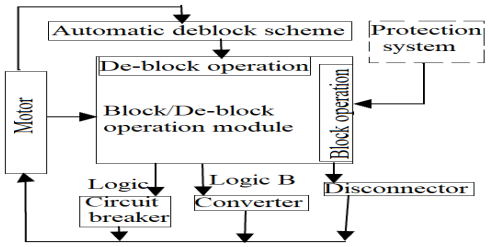


Fig. 6: Inverter restoration strategy.

V. INVERTER BLOCKING/DE-BLOCKING METHOD

The block and de-block operation orders to the converter are generated by the block/de-block module as depicted in Fig. 8. The block/de-block module comprises of 4 input and 2 output, where the input (a) is the state of opening the grid circuit breaker when the state is low or zero, the input (b) is the event to de-block the converter after the closing of the circuit breaker by the AND gate, the input (c) is the event to block the converter when receives an unwanted signal such as over-voltage or a fault current which will reset the Set-Reset (SR) trigger and the Q will goes to zero or low state thereby open the circuit breaker. The reset input, reset the device to its original state with an output Q which will be either at high level 1 or low level 0 depending on the set/reset condition. The SR logic is one-bit bistate device which has 2 inputs known as set and reset. The device is Set (S) when the output is 1and Reset (R) when the output is zero (0). The blocking of the converter is vital to the grid switching devices protection from fault current, voltage rise and under-voltage. At the clearing of the grid fault event, the converter is de-block to restore power. When de-block signal is received by the converter, the circuit breaker will turn off before the converter de-block. The input (d) is any fault occurrence that may occur from the DC side.

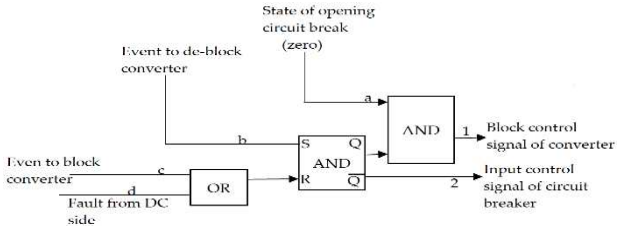


Fig. 8: Converter Block/De-block module strategy.

TABLE 1: OR GATE TRUTH TABLE

OR Gate			AND Gate							
Input		Output	Input		Output	S	R	Q	$\bar{Q}$	Description
A	B	Y = A+B	A	B	Y = A. B	1	0	0	1	Set $\bar{Q}$ = 1
0	0	0	0	0	0	1	1	0	1	No change
0	1	1	0	1	0	0	1	1	0	Set $\bar{Q}$ = 0
1	0	1	1	0	0	1	1	1	0	No change
1	1	1	1	1	1	0	0	1	1	invalid

VI. NETWORK DESCRIPTION

Solar panel of 330, 100.7 kW is connected into the 100 kVA, 260/25 kV distribution network via inverter to detect the MPP using IIC & IR method. As depicted in Fig. 11, the blocking and deblocking process modules are integrated into the inverter to create blocking and de-blocking signal sequences for the inverter. The PV consists of two inputs, i.e., temperature o^c and the irradiance in W/m^2). The inverter is a three-phase, three-level Voltage Source Converter (VSC) with internal and external control techniques. The PV temperature and irradiation properties are attained at 25^{0}C and 1000W/m^2. The system enhances from 273 to 500 V DC at device maximum output. To obtain maximum output, the algorithm adjusts considerably and enhances the duty cycle of the inverters. The voltage source converter maintains the power factor at 1 by adjusting I_q to zero and converting the DC voltage link from 500 V DC to 260 V AV. To reduce distortions caused by the inverter, a 10 kVAR filtering circuit is connected to the VSC output.

VII. SIMULATION, RESULT AND DISCUSSION

The network is simulated for 3 s, at the sample time (t) equal to 0.05 s, blocking signals are applied to the inputs of both boost converter and three level voltage source converters as shown in Figure 9 to block the converter from unwanted signals such as switch-on instantaneous input current surge drawn by an electrical device connected to the grid when first turned on. It is observed between 0 to 0.05 s that the converter operates as rectifier and the direct current link capacitors are charged to about 590 V as depicted in Fig. 10 while the solar voltage obtained is 320.986 V in Fig. 11 which should be equal to the open circuit voltage. By calculation using eqn. (17), the solar voltage is 321 V, where ($PV_{voltage}$) is the solar voltage, (N_{series}) is the no of series solar module and (V_{oc}) is the open circuit voltage. The value got for the solar voltage by calculation, is approximately equal to the value obtained from the simulation graph as shown in Fig. 13. At t = 0.05 s, both boost converter and voltage source converter are de-blocked as depicted while the duty cycle of the boost converter is fixed at D = 0.5 as depicted in Fig. 11. The direct current link voltage is controlled and maintained steady state of 500.64 V at t = 0.205 s. The solar steady state voltage is obtained in (20) by calculation, where (D) and (V_{dc}) are the duty circuit and the direct current link voltage. The calculated steady state voltage is 250.32 V in eqn. (19) which is approximately agreed with the simulated value 249.5447 V in Fig. 13. The grid current and voltage is kept at unity power factor such that they are in phase,

the solar and the grid output power produced 95.3199 kW and 93. 5221 kW respectively in Fig. 14. Although, the specific power rating of the solar is 100.7 kW with Irradiance of 1000 W/m^2.

$$PV_{voltage} = N_{series} \times V_{oc} \quad (15)$$

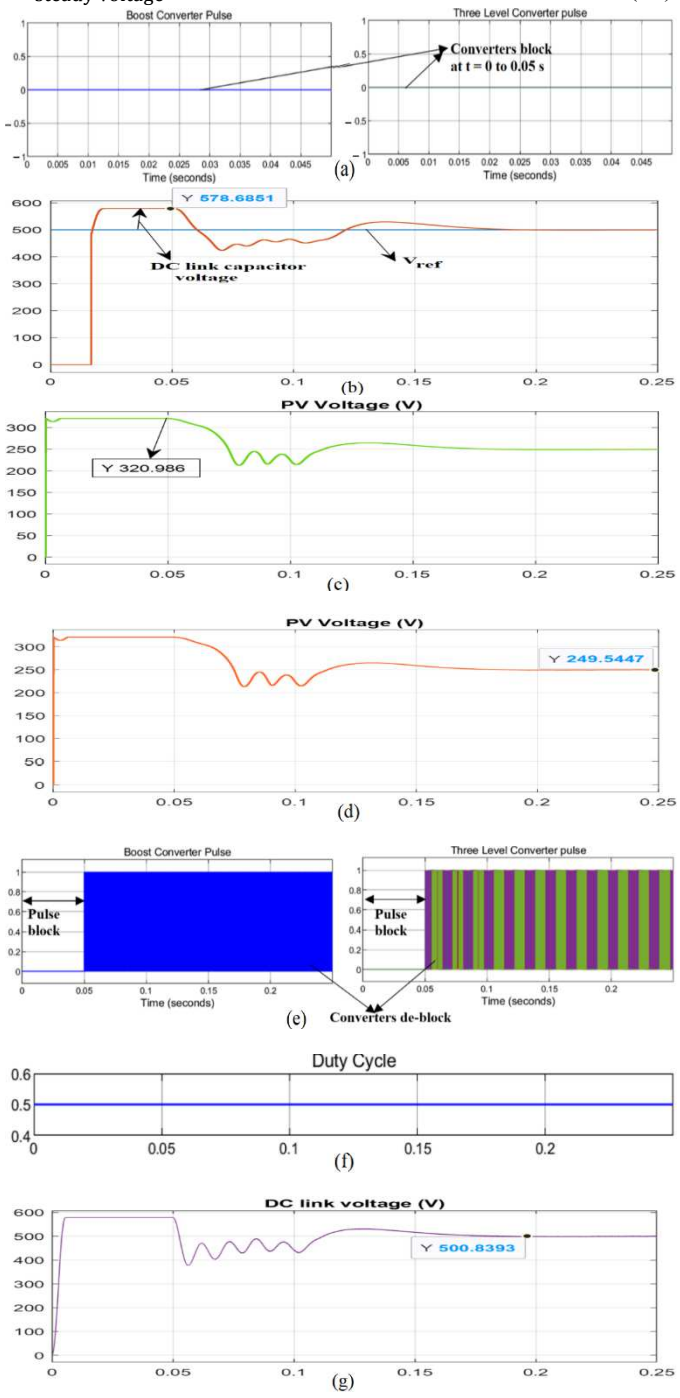
$$PV_{voltage} = 5 \times 64.2 \quad (16)$$

$$PV_{voltage} = 321\ V \quad (17)$$

$$PV_{steady\ voltage} = (1 - D) \times Vdc \quad (18)$$

$$PV_{steady\ voltage} = (1 - 0.5) \times 500.64 \quad (19)$$

$$PV_{steady\ voltage} = 250.32\ V \quad (20)$$



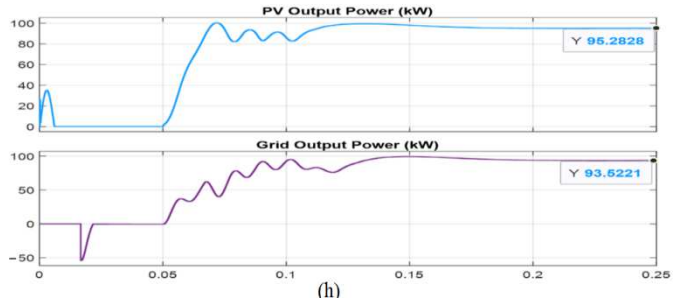


Fig. 8: (a) Inverter blocking (b) DCLC and reference voltage (c) PV voltage equivalent to OCV (d) Inverter deblocking (e) BI duty cycle (f) Regulated DCLC voltage (g) PV output voltage and power (h) PV and Grid output power.

PPT is allowed at t = 0.59 s. The simulation results for PV output power and voltage, grid output power, and duty cycle are shown in Fig. 9a. PPP regulator starts the regulation at t = 0.4 s by controlling and varying the duty cycle to extract the peak power, The PV produces 101 kW while the grid produces 99.1 kW, the PV voltage increase from 250.9 V to 272.900 V at t = 0.419 s and remains stable until t = 0.59 s. The duty cycle increases to 0.43902 and remains stable at 0.44922. Eq. 21 is used to make comparisons the simulated results of PV output voltage in Fig. 9a with the PV modules configuration. The controller reduces the error to zero at t = 0.419 s, as depicted in Fig. 9b.

$$\text{Solar output specification} = N_{ser} \times \text{Voltage} \quad (21)$$

$$\text{solar output specification} = 5 \times 54.7 \quad (22)$$

$$273.5\ V \quad (23)$$

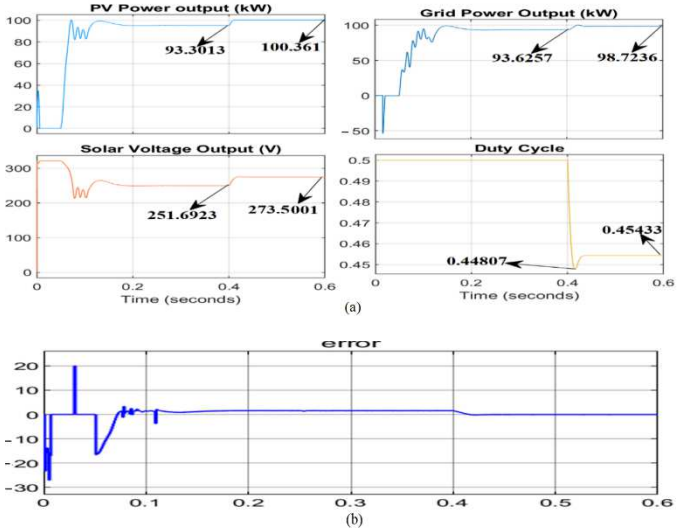
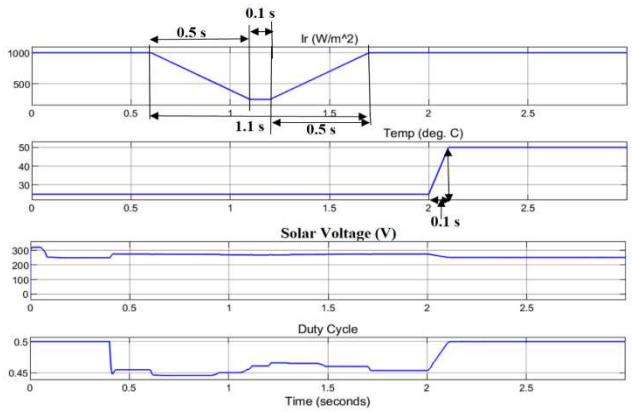


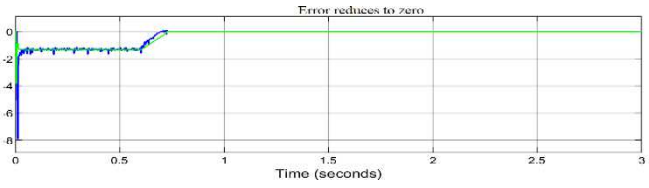
Fig. 9: (a) PPPT Tracking (b) Regulator lowers error to zero at t = 0.4 s

Fig. 10a depicts a transition in irradiance at t = 1.49 s. At t = 0.6119 s, the sun's irradiance varies unexpectedly within 0.49 s and then stabilizes for 0.1 s. In the same Fig. 10a, irradiance

subsequently varies from 2499 W/m^2 to 690. W/m^2 in 0.49 s, the temperature maintained at 25 degrees, and the duty cycle continues to vary and stabilize at D = 0.4700. The fluctuation in PV irradiation indicated a decrease in PV and grid output power; the photovoltaic output power altered within 0.5 s from 101 W to 24.9 kW and eventually to 70 kW, whereas the grid output power altered within 0.6 s from 99 kW to 27.9 kW and ultimately to 66 kW, while the temperature remained constant at 24.9 degrees. At t = 3 s, the sun's irradiation is recovered from 250.9 W/m^2 to 999.9 W/m^2 within 0.45 s, while the temperature rises from 24.9 to 49.9 degrees within 0.45 s, as shown in the same Fig 10a. The maximum time of the transition in sun irradiation is 1.09 s, and the output power is reduced throughout this time, but the MPP tracking algorithm continues to detect the maximum output and the solar voltage output remains constant. The integra controller reduces the error produced to zero in Fig 10b; a voltage dip occurs on the boost converter side, but the voltage on the 3-level inverters side remains constant despite variations in sun irradiation. The 3-level inverter avoids voltage dips in the grid, keeps power quality within an allowable threshold, and keeps load current very low during the transition in sun irradiation duration, as shown in Fig. 10c. This simulation demonstrates that photovoltaic output power may alter abruptly due to an unexpected variation in PV irradiation caused by deflection of the incoming beam, clouds, airborne aerosols, snow, ice, and ground surface reflectivity, but with a BI, 3-level inverters, and application of IR with PPP detector, satisfactory grid voltage and steady PVSS voltage output will therefore be assured.



(a)



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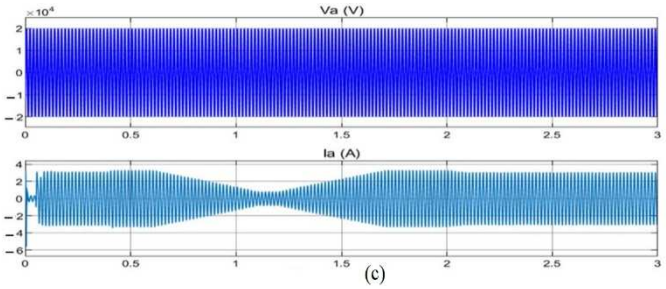

(c)

Fig. 10: (a) Irradiance, Temperature, PVSS Voltage, Duty cycle and IR (b) Error tends to zero (c) Network Voltage and Current.

VIII. CONCLUSION

This paper presents an AIC & IR for obtaining maximum power output from a PVSS. The proposed method achieves outstanding and correct results in detecting peak power output from solar panels, while preserving and enhancing generated output voltage despite the weather variability. As a result, controller controls and reduces oscillations/errors caused by PPP voltage and the sliding surface.

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